an electrical insulation configured to surround said superconducting material, wherein said electrical insulation including

an inner layer of semiconducting material electrically connected to said superconductor,

an outer layer of semiconducting material held at a controlled electric potential along a length of said outer layer of semiconducting material, and

an intermediate layer of a solid electrically insulating material positioned between said inner layer of semiconducting material and said outer layer of semiconducting material.

38. The SMES device according to claim 37, further comprising:

a cryostat configured to enclose said coil and said switch.

39. The SMES device according to claim 37, wherein said superconductor comprises:

a high-temperature superconductor.

40. The SMES device according to claim 39, wherein said high-temperature superconductor comprises:

at least one layer of high-temperature superconducting material;

a cooler configured to cryogenically cool said at least one layer of high-temperature superconducting material below said critical temperature; and

a thermal insulator configured to surround said at least one layer of high-temperature superconducting material and said cooler.

41. The SMES device according to claim 40, wherein said cooler comprises:

a support tube through which a cryogenic cooling fluid is passed and about which said at least one layer of high-temperature superconducting material is wound as a tape in a helical layer.

42. The SMES device according to claim 40, wherein said cooler comprises:

a support tube through which a cryogenic cooling fluid is passed and about which said at least one layer of high-temperature superconducting material is wound as a plurality of conductors in a helical layer.

43. The SMES device according to claim 40, wherein said thermal insulator comprises:

an annular space under vacuum containing a thermal insulation.

44. The SMES device according to claim 37, wherein said outer layer of semiconducting material having a resistivity in an inclusive range from 1 through 1000 ohm-cm.

45. The SMES device according to claim 43, wherein said outer layer of semiconducting material having a resistivity in an inclusive range from 10 through 500 ohm-cm.

46. The SMES device according to claim 43, wherein said outer layer of semiconducting material having a resistivity in an inclusive range from 10 through 100 ohm-cm.

47. The SMES device according to claim 37, wherein said outer layer of semiconducting material having a resistance per axial unit length in an inclusive range from 5 through 50,000 ohm-$m^{-1}$.

48. The SMES device according to claim 37, wherein said outer layer of semiconducting material having a resistance per axial unit length in an inclusive range from 500 through 25,000 ohm-$m^{-1}$.

49. The SMES device according to claim 37, wherein said outer layer of semiconducting material having a resistance per axial unit length in an inclusive range from 2,500 through 5,000 ohm-$m^{-1}$.

50. The SMES device according to claim 37, wherein said outer layer of semiconducting material being contacted by a conductor at said controlled electric potential at a plurality of separated regions along said length of said outer layer of semiconducting material such that adjacent regions of said plurality of separated regions being sufficiently close together that a plurality of mid-point voltages between said adjacent regions being insufficient to cause a corona discharge to occur within said electrical insulator.

51. The SMES device according to claim 37, wherein said controlled electric potential being substantially an earth potential.

52. The SMES device according to claim 37, wherein said intermediate layer being in close mechanical contact with said inner layer of semiconducting material and said outer layer of semiconducting material.

53. The SMES device according to claim 37, wherein said intermediate layer being joined to said inner layer of semiconducting material and said outer layer of semiconducting material.

54. The SMES device according to claim 37, wherein a strength of adhesion between said intermediate layer and said inner layer of semiconducting material and said

outer layer of semiconducting material being greater than one tenth and less than ten times an intrinsic strength of said solid electrically insulating material of said intermediate layer.

55. The SMES device according to claim 53, wherein said intermediate layer, said inner layer of semiconducting material, and said outer layer of semiconducting material being joined together by extrusion.

56. The SMES device according to claim 55, wherein said intermediate layer, said inner layer of semiconducting material, and said outer layer of semiconducting material being applied together over said superconductor via a multi-layer extrusion die.

57. The SMES device according to claim 37, wherein:

said inner layer of semiconducting material including a first plastic material having a first plurality of electrically conductive particles dispersed therein; and

said outer layer of semiconducting material including a second plastic material having a second plurality of electrically conductive particles dispersed therein; and

said solid electrically insulating material of said intermediate layer including a third plastic material.

58. The SMES device according to claim 57, wherein said first plastic material, said second plastic material, and said third plastic material comprise:

at least one of an ethylene butyl acrylate copolymer rubber, an ethylene-propylene-diene monomer rubber, an ethylene-propylene copolymer rubber, a LDPE, a HDPE, a PP, a PB, a PMB, a XLPE, an EPR, and a silicone rubber.

59. The SMES device according to claim 57, wherein said first plastic material, said second plastic material, and said third plastic material having a substantially identical coefficient of thermal expansion.

60. The SMES device according to claim 57, wherein said first plastic material, said second plastic material, and said third plastic material being a substantially identical material.

61. The SMES device according to claim 37, wherein said SMES device being connected to a high voltage source and forming an electric power transmission system.

62. A high voltage system, comprising:

an SMES device having a superconductor insulated against a high voltage by an electric insulation system arranged concentrically around said superconductor.

63. The high voltage system according to claim 62, wherein said high voltage system further comprises:

a high voltage network directly connected to said SMES device without an intermediate transformer.

64. The high voltage system according to claim 63, wherein said high voltage network comprises a high voltage DC network.

65. The high voltage system according to claim 64, wherein said high voltage DC network being configured to operate at a voltage exceeding 10 kV.

66. The high voltage system according to claim 63, further comprising:

a converter configured to couple said SMES device to a high voltage AC network.

67. The high voltage system according to claim 64, further comprising:

a plurality of AC networks connected via said DC network and said SMES device, wherein said DC network being connected to said plurality of AC networks so that said SMES device provides said plurality of AC networks with power.

68. The high voltage system according to claim 62, wherein said SMES device comprises:

a coil.

69. The high voltage system according to claim 62, wherein said SMES device comprises:

a cable without turns.

70. The high voltage system according to claim 66, wherein said SMES forming a part of a bipolar DC link.

71. The high voltage system according to claim 62, wherein said insulation system comprises:

a first integral semiconducting part configured to form an inner layer in electric contact with said superconductor;

a second integral semiconducting part configured to form an outer layer around an insulating integral third part; and

said insulating integral third part between said first integral semiconducting part and said second integral semiconducting part;

wherein said insulation system being extruded around said superconductor.

72. The high voltage system according to claim 62, wherein said insulation system comprises:

an all-synthetic semiconducting film wound in an overlapping layer around said superconductor with an inner part of said all-synthetic film in electric contact with said superconductor;

an electrically insulating intermediate part; and

an outer semiconducting part surrounding said electrically insulating intermediate part.

Sub B3 73. The high voltage system according to claim 62, wherein said insulation system comprises:

at least one of a cellulose-based, synthetic paper and a non-woven fibre material being co-lapped with a synthetic film and including

an inner semiconducting part in electric contact with said superconductor,

an electrically insulating intermediate part, and

an outer semiconducting part around said electrically insulating intermediate part.

74. The high voltage system according to claim 62, wherein said insulation system comprises:

at least one of a cellulose-based, synthetic paper and a non-woven fibre material being laminated with a synthetic film and including

an inner semiconducting part in electric contact with said superconductor,

an electrically insulating intermediate part, and

an outer semiconducting part around said electrically insulating intermediate part.

75. The high voltage system according to claim 71, further comprising:

a cooling medium configured to cool said superconductor through flow within said superconductor.

76. The high voltage system according to claim 72, further comprising:

a cooling medium configured to cool said superconductor through flow within said superconductor.

77. The high voltage system according to claim 71, further comprising:

a cooling medium configured to cool said superconductor arranged outside of said superconductor.

78. The high voltage system according to claim 72, further comprising:

a cooling medium configured to cool said superconductor arranged outside of said superconductor.

79. An SMES device comprising:

a switch configured to short circuit a coil; and

said coil configured to be connected in series with a voltage source and wound from a superconducting cable, said coil including

means for superconducting maintained at cryogenic temperatures below a critical temperature during use, and

means for electrically insulating said means for superconducting, including

an inner layer of a semiconducting material electrically connected to said means for superconducting,

an outer layer of semiconducting material held at a controlled electric potential along a length thereof, and

an intermediate layer of a solid electrical insulation positioned between said inner layer and said outer layer.

**IN THE ABSTRACT OF THE DISCLOSURE**

After the last page of the Specification, please insert the following: